UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,793	02/02/2000	Farooq Jabbar	60705-1210	6699

7590 05/01/2003

Daniel R McClure
Thomas Kayden Horstemeyer & Risley LLP
100 Galleria Parkway NW
Suite 1500
Atlanta, GA 30339-5948

EXAMINER
ODOM, CURTIS B

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 05/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/496,793	JABBAR ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 28-30 are objected to because of the following informalities: On line 1, the word "method" is suggested to be changed to "system". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3-13 and 19-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Aslanis et al. (U.S. Patent No. 5, 627, 863).

Regarding claim 3, Aslanis et al. discloses a method for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

receiving (Fig. 1, block 12, column 3, lines 60-66) and column 5, lines 15-16) a plurality of signals generated and transmitted by an associated far-end transmission unit;

converting (Fig. 1, block 32, column 5, lines 15-19) the plurality of received signals through an ADC;

detecting (Fig. 1, block 50, column 6, lines 19-27) a phase error on the received pilot tone;

applying (Fig. 1, blocks 52 and 46, column 6, lines 13-19 and 23-27) the phase error to a phase locked-loop to generate a frequency correction signal; and

using (Fig. 1, block 46, column 6, lines 13-19) the frequency correction signal to modify the sampling time of the ADC.

Regarding claim 4, Aslanis et al. discloses the method of claim 3, wherein the detection of phase error is compensated by an offset based on the received signal segment in the initialization sequence (column 5, lines 59-67 and column 6, lines 19-27), wherein frame synchronization is an initialization process (column 1, lines 59-67 and column 2, lines 1-3).

Regarding claim 5, Aslanis et al discloses the method of claim 3, wherein the step of detecting a phase error is performed with a state machine in communication with the ADC output and the input to the PLL (Fig. 1, block 50, column 6, lines 19-27), wherein the phase comparator is a state machine in that it detects a phase error.

Regarding claim 6, Aslanis et al. discloses a method of claim 3, further comprising synchronizing a DAC in the transmitting path by using a sampling clock derived from the PLL controlled ADC (column 5, lines 46-60).

Regarding claim 7, Aslanis et al. discloses a method for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

receiving (Fig. 1, block 12, column 3, lines 60-66, column 5, lines 15-16 and 56-60 and column 6, lines 3-12) a pilot tone generated and transmitted along with other signal streams at a particular receiver;

converting (Fig. 1, block 32, column 5, lines 15-19) the plurality of received signals through an ADC to create a digital signal stream;

detecting (Fig. 1, block 34, column 5, lines 19-23) the cyclic prefix in the received digital signal stream;

zeroing out (Fig. 1, block 36, column 5, lines 23-27) the received digital signal stream from the input to a PLL while the cyclic prefix is present in the received signal stream to create a frequency correction signal, wherein removing the cyclic prefix from the received digital stream zeroes out the received digital stream; and

using (column 6, lines 13-27) the frequency correction signal to modify the ADC sampling time.

Regarding claim 8, Aslanis et al. discloses the method of claim 7, further comprising synchronizing a DAC in the transmitting path by using a sampling clock derived from the PLL controlled ADC (column 5, lines 46-60).

Regarding claim 9, Aslanis et al. discloses a method for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

receiving (Fig. 1, block 12, column 3, lines 60-66, column 5, lines 15-16 and 56-60 and column 6, lines 3-12) a standard pilot tone generated and transmitted by an associated far-end transmission unit along with other signal streams at a particular receiver;

converting (Fig. 1, block 32, column 5, lines 15-19) the plurality of received signals through an ADC to create a digital signal stream;

detecting (Fig. 1, block 34, column 5, lines 19-23) the cyclic prefix in the received digital signal stream;

performing (Fig. 1, block 34, column 5, lines 15-23) a time-domain equalization on the received signal stream;

removing (Fig. 1, block 36, column 5, lines 23-27) the cyclic prefix portion of the equalized digital signal stream from the input to a PLL to create a frequency correction signal; and

using (column 6, lines 13-27) the frequency correction signal to modify the ADC sampling time.

Regarding claim 10, Aslanis et al. discloses the method of claim 9, further comprising synchronizing a DAC in the transmitting path by using a sampling clock derived from the PLL controlled ADC (column 5, lines 46-60).

Regarding claim 11, Aslanis et al. discloses a method for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

receiving (Fig. 1, block 12, column 3, lines 60-66, column 5, lines 15-16 and 56-60 and column 6, lines 3-12) a standard pilot tone generated and transmitted by an associated far-end transmission unit along with other signal streams at a particular receiver;

converting (Fig. 1, block 32, column 5, lines 15-19) the plurality of received signals through an ADC to create a digital signal stream;

detecting (Fig. 1, block 34, column 5, lines 19-23) the cyclic prefix in the received digital signal stream;

using (Fig. 1, block 38, lines 27-31) the equalized signal stream with the cyclic prefix portion removed to estimate the phase error with a DFT;

applying (column 6, lines 19-23) the estimated phase error to the input of a PLL to create a frequency correction signal; and

using (column 6, lines 13-27) the frequency correction signal to modify the ADC sampling time.

Regarding claim 12, Aslanis et al. discloses the method of claim 11, further comprising synchronizing a DAC in the transmitting path by using a sampling clock derived from the PLL controlled ADC (column 5, lines 46-60).

Regarding claim 13, Jenness does not disclose the method of claim 1 configured into a DSP. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the steps of claim 1 into a DSP rather than individual devices to perform each step because this would save cost and simplify implementation. Therefore, claim 13 does not constitute patentability.

Regarding claim 19, Aslanis et al. discloses a system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

an ADC (Fig. 1, block 32, column 5, lines 15-19);

a state machine (Fig. 1, block 50, column 6, lines 19-27) in communication with the ADC configured to determine the phase offset on a pilot tone in a received signal segment; and

a phase locked loop (Fig. 1, blocks 46 and 52, column 5, lines 13-27) in configured to compensate for the phase offset and to apply a control signal to the ADC, wherein the received signal samples are synchronized for further processing at a rate compatible with that of a source transmission.

Regarding claim 20, Aslanis et al. discloses the system of claim 19, further comprising:

a sampling clock (Fig. 1, line 44, column 5, lines 46-60 and column 6, lines 13-17) in communication with the ADC, the sampling clock in further communication with a DAC in an upstream data path for synchronizing data transmitted in an upstream direction to the source.

Regarding claim 21, Aslanis et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

an ADC (Fig. 1, block 32, column 5, lines 15-19) configured to create a digital representation of the received signal;

a phase locked loop (Fig. 1, blocks 46 and 52, column 5, lines 13-27) in communication with the ADC configured to receive the received signal to apply a control signal to the ADC, wherein the received signal sample stream is synchronized for further processing at a rate compatible with that of a source transmission; and

a symbol synchronizer (Fig. 1, block 36, column 5, lines 23-27) in communication with the ADC configured to determine when the data stream contains a cyclic prefix, the symbol synchronizer configured to remove the received signal from the PLL input when the cyclic prefix is present, wherein removal of the cyclic prefix by the buffer from the received signal removes the received signal from the PLL input so that the PLL can process the received signal without the cyclic prefix.

Regarding claim 22, Aslanis et al. discloses the system of claim 21, further comprising:

a sampling clock (Fig. 1, line 44, column 5, lines 46-60 and column 6, lines 13-17) in communication with the ADC, the sampling clock in further communication with a DAC in an upstream data path for synchronizing data transmitted in the reversed direction to the far-end transmission unit.

Regarding claim 23, Aslanis et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

an ADC (Fig. 1, block 32, column 5, lines 15-19) configured to create a digital representation of the received signal;

an equalizer (Fig. 1, block 34, column 5, lines 15-23) in communication with ADC configured to perform a time-domain equalization on the received signal;

a phase locked loop (Fig. 1, blocks 46 and 52, column 5, lines 13-27) in communication with the ADC configured to receive the received signal to apply a control signal to the ADC, wherein the received signal sample stream is synchronized for further processing at a rate compatible with that of a source transmission; and

a symbol synchronizer (Fig. 1, block 36, column 5, lines 23-27) in communication with the ADC configured to determine when the signal stream contains a cyclic prefix, the symbol synchronizer configured to remove the time-domain equalized signal from the PLL input when the cyclic prefix is present, wherein removal of the cyclic prefix by the buffer from the received signal removes the time-domain equalized signal from the PLL input so that the PLL can process the time-domain equalized signal without the cyclic prefix.

Regarding claim 24, Aslanis et al. discloses the system of claim 23, further comprising:

a sampling clock (Fig. 1, line 44, column 5, lines 46-60 and column 6, lines 13-17) in communication with the ADC, the sampling clock in further communication with a DAC in an upstream data path for synchronizing data transmitted in the reversed direction to the far-end transmission unit.

Regarding claim 25, Aslanis et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

an ADC (Fig. 1, block 32, column 5, lines 15-19) configured to create a digital representation of the received signal;

an equalizer (Fig. 1, block 34, column 5, lines 15-23) in communication with ADC configured to perform a time-domain equalization on the received signal;

a DFT (Fig. 1, block 38, column 5, lines 27-31) in communication with the equalizer, the DFT configured to convert the time-equalized received signal and to generate a pilot tone phase error estimate signal;

a symbol synchronizer (Fig. 1, block 36, column 5, lines 23-27) in communication with the ADC configured to remove the cyclic prefix from the signal sample stream; and

a phase locked loop (Fig. 1, blocks, 46 and 52, column 5, lines 13-27) in communication with the ADC and DFT configured to receive pilot tone phase error estimate and to apply a control signal to the ADC, wherein the received signal sample stream is synchronized for further processing at a rate compatible with that of a source transmission.

Regarding claim 26, Aslanis et al. discloses the system of claim 27, further comprising:

a sampling clock (Fig. 1, line 44, column 5, lines 46-60 and column 6, lines 13-17) in communication with the ADC, the sampling clock in further communication with a DAC in an upstream data path for synchronizing data transmitted in the reversed direction to the far-end transmission unit.

Regarding claim 27, Aslanis et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

means for receiving (Fig. 1, block 12, column 3, lines 60-66, column 5, lines 15-16 and 56-60 and column 6, lines 3-12) a pilot tone generated and transmitted by an associated far-end transmission unit;

means for converting (Fig. 1, block 32, column 5, lines 15-19) the received pilot tone along with other received signals from an analog to a digital signal;

means for detecting (Fig. 1, block 50, column 6, lines 19-27) a phase error on the received pilot tone;

means for applying (Fig. 1, blocks 52 and 46, column 6, lines 13-19 and 23-27) the phase error to a phase locked-loop to generate responsive to when the cyclic prefix is not present in the digital signal; and

means for using (Fig. 1, block 46, column 6, lines 13-19) the output signal to modify the ADC timing.

Regarding claim 28, Aslanis et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

means for receiving (Fig. 1, block 12, column 3, lines 60-66, column 5, lines 15-16 and 56-60 and column 6, lines 3-12) a standard pilot tone and far-end signal from an associated far-end transmission;

means for converting (Fig. 1, block 32, column 5, lines 15-19) the plurality of received signals from analog to digital signals;

means for detecting (Fig. 1, block 34, column 5, lines 19-23) the cyclic prefix in the received far-end signal;

means for removing (Fig. 1, block 36, column 5, lines 23-27) the cyclic prefix in the received far-end signal;

means for estimating (Fig. 1, block 38, lines 27-31) the phase error in the pilot tone with a DFT;

means for applying (column 6, lines 19-23) the estimated phase error to the input of a PLL to create a frequency correction signal; and

means for using (column 6, lines 13-27) the frequency correction signal to modify the ADC sampling rate.

Regarding claim 29, Aslanis et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

means for receiving (Fig. 1, block 12, column 3, lines 60-66, column 5, lines 15-16 and 56-60 and column 6, lines 3-12) a standard pilot tone with a plurality of signals at this particular receiver from a far-end signal;

means for converting (Fig. 1, block 32, column 5, lines 15-19) the plurality of signals from analog to digital signals;

means for performing (Fig. 1, block 34, column 5, lines 15-23) a time-domain equalization on the far-end signal;

means for detecting (Fig. 1, block 34, column 5, lines 19-23) the cyclic prefix in the far-end signal;

means for zeroing out (Fig. 1, block 36, column 5, lines 23-27) the equalized digital signal from the input to a PLL while the cyclic prefix is present in the received signal to create a

frequency correction signal, wherein removing the cyclic prefix from the received digital signal zeroes out the equalized digital signal; and

means for using (column 6, lines 13-27) the frequency correction signal to modify the ADC sampling rate.

Regarding claim 30, Aslanis et al. discloses system for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

means for receiving (Fig. 1, block 12, column 3, lines 60-66, column 5, lines 15-16 and 56-60 and column 6, lines 3-12) a far-end signal along with a plurality of signals at the receiver;

means for converting (Fig. 1, block 32, column 5, lines 15-19) the plurality of received signals from an analog to digital format;

means for detecting (Fig. 1, block 34, column 5, lines 19-23) the cyclic prefix in the far-end signal;

means for zeroing out (Fig. 1, block 36, column 5, lines 23-27) the far-end signal when the cyclic prefix is present from the input to a PLL, wherein removing the cyclic prefix from the received digital signal zeroes out the far-end signal; and

means for using the PLL output (column 6, lines 13-27) to modify the ADC sampling rate.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenness (U.S. Patent No. 6, 404, 774).

Regarding claim 1, Jenness discloses a method for reducing pilot tone phase interference at the transmitter in a DMT communications system (column 1, lines 48-52) comprising:

generating DMT signal segments REVERB (column 13, lines 24-46) and SEGUE (column 14, lines 23-35);

and transmitting (column 13, lines 24-46 and column 14, lines 23-35) the above-defined REVERB and SEGUE signals in the DMT initialization sequence.

Jenness does not disclose the segments are generated using pseudo-random pattern generator using an initial pattern that minimizes pilot tone phase offsets.

However Jenness does disclose that the REVERB segment is a pseudo-random signal which is used to detect SNR and can be transmitted at a known amplitude and can be designed to optimize transmission amplitude. This segment can be used to track the noise and amplitude for each tone channel (column 13, lines 47-50). Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made that a pseudo-random pattern generator could have been implemented into the communications system since the segment is a pseudo-random signal and since the an initial pattern is designed by the user and can be used to optimize transmission amplitude, then an initial pattern could also be designed by the user to minimize a phase offset by choosing a phase for the segment at transmission that would minimize the phase offset at the receiver.

Regarding claim 2, which inherits the limitations of claim 1, Jenness discloses generating ADSL-over-POTS DMT signal segments C-REVERB (column 13, lines 24-46) and C-SEGUE (column 14, lines 23-35) as defined by the ADSL standard; and

transmitting (column 13, lines 24-46 and column 14, lines 23-35) the C-REVERB and C-SEGUE signal in the DMT ADSL standard initialization sequence.

Jenness does not disclose using a pseudo-random pattern generator polynomial with an initial pattern of 30 (0x05 A).

However, Jenness discloses that the REVERB segment is a pseudo-random signal which is used to detect SNR and can be transmitted at a known amplitude and can be designed to optimize transmission amplitude. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a pseudo-random pattern generator could have been implemented into the communications system since the segment is a pseudo-random signal and that since the user designs the initial pattern of the segments that the segments can be designed using an initial pattern of 90 (0x05A).

6. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aslanis et al. (U.S. Patent No. 5, 627, 863).

Regarding claim 14, Aslanis et al. discloses a device configured to compensate for the offset in phase error on a received pilot tone based upon the received signal segment in the DMT system initialization sequence (Fig. 1, block 12, column 6, lines 13-27). Aslanis et al does not disclose the device is a DSP.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the device into a DSP rather than individual devices to perform each step of the phase compensation because this would save cost in building the device and simplify implementation of the device. Therefore, configuring the device into a DSP does not constitute patentablitiy.

Regarding claim 15, which inherits the limitations of claim 14, Aslanis et al. further discloses the phase error compensation is accomplished with a phase comparator (Fig. 1, block 50, column 6, lines 19-27). Aslanis et al. does not disclose the phase error compensation is accomplished by a state machine. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that since the state machine is also used for phase error compensation that it could have been implemented in place of the phase comparator. Thus, a state machine used to compensate for phase error is deemed a design choice and does not constitute patentability.

Regarding claim 16, Aslanis et al discloses a device to detect and zero out the cyclic prefix from a received digital stream when the cyclic prefix is present to create an input to a PLL (Fig. 1, block 12, column 5, lines 19-27). Aslanis et al does not disclose the device is a DSP.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the device into a DSP rather than individual devices to

perform each step of the detection and zeroing out of the cyclic prefix because this would save cost in building the device and simplify implementation of the device. Therefore, configuring the device into a DSP does not constitute patentablitiy.

Regarding claim 17, which inherits the limitations of claim 16, Aslanis et al. further discloses performing a time-domain equalization on a received digital data stream and creating an input to a PLL when the cyclic prefix is zeroed out from the signal stream (column 5, lines 15-27).

Regarding claim 18, Aslanis et al discloses a device configured to detect and remove the cyclic prefix from a received digital stream when the cyclic prefix is present, the device further configured to first perform a time-domain equalization of the digital signal stream, then to perform a discrete Fourier transform on the digital signal stream when the cyclic prefix is not present to create a phase error signal for application at the input to a PLL (Fig. 1, block 12, column 5, lines 15-31). Aslanis et al does not disclose the device is a DSP.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the device into a DSP rather than individual devices to perform each step of the process because this would save cost in building the device and simplify implementation of the device. Therefore, configuring the device into a DSP does not constitute patentablitiy.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 703-305-4097. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Curtis Odom
April 22, 2003

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600